FIG. 1

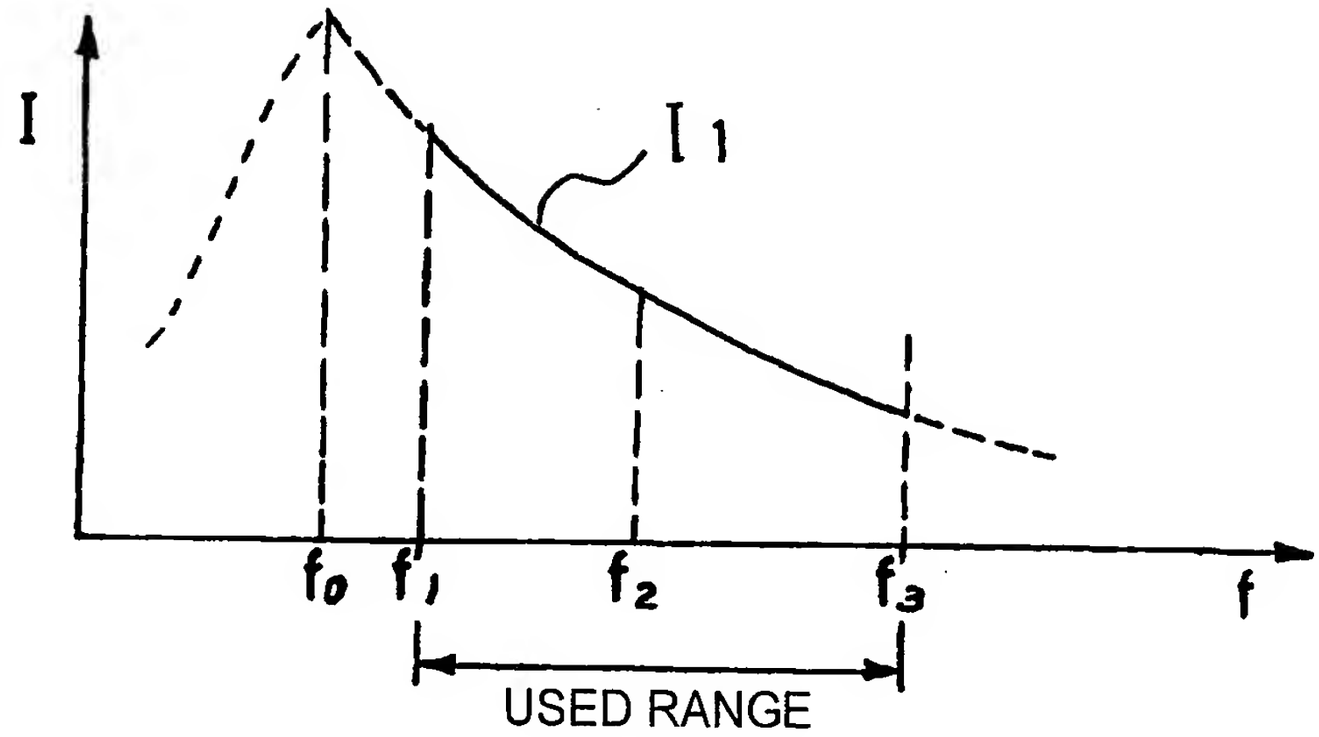


FIG. 2

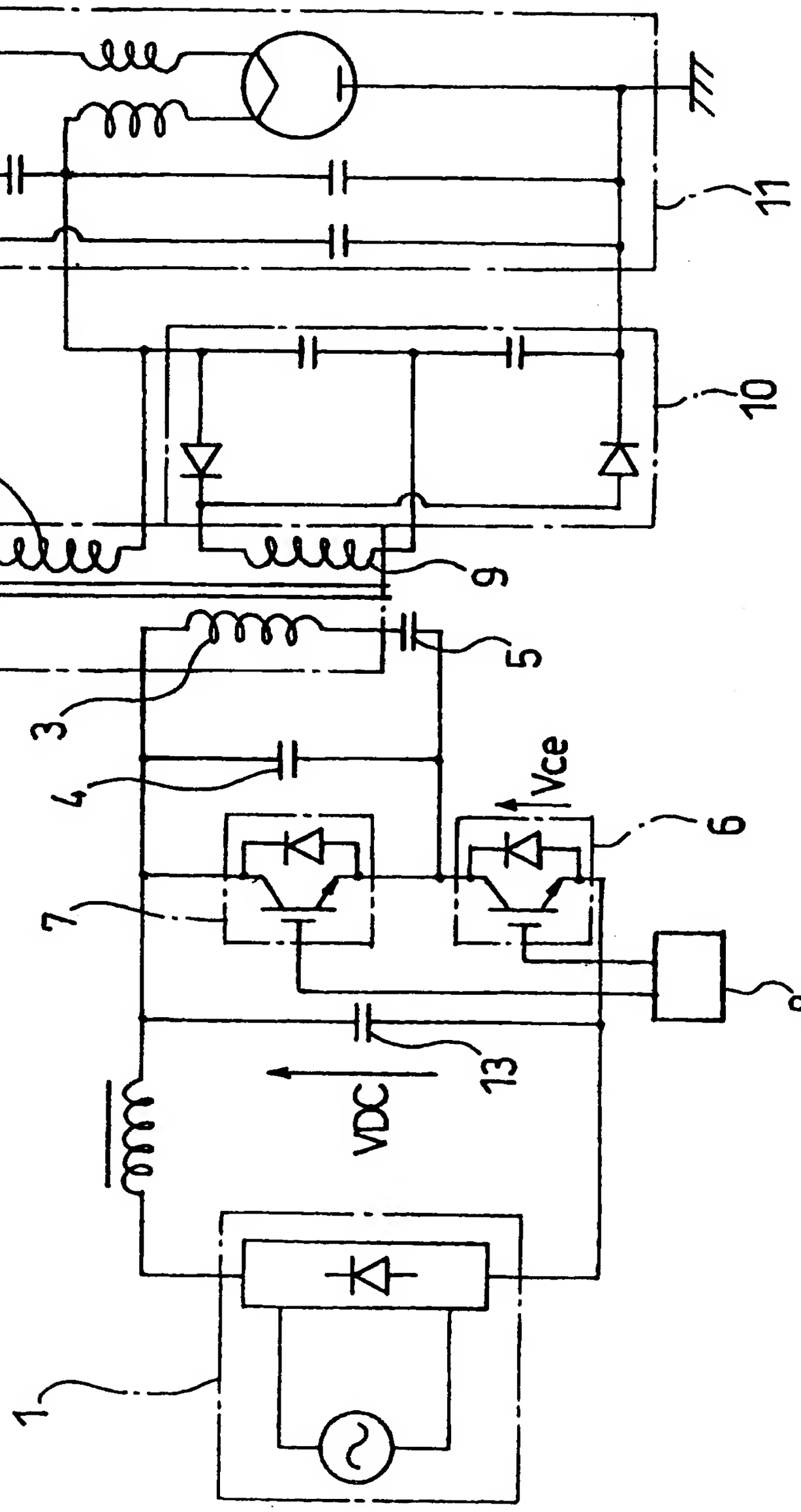


FIG. 3 (a)

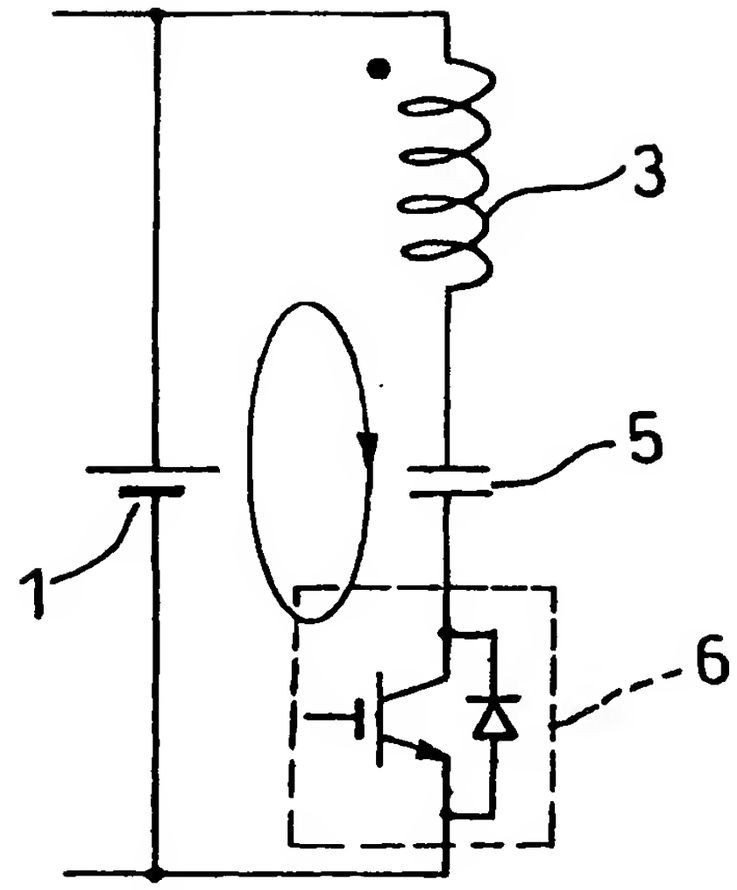


FIG. 3 (b)

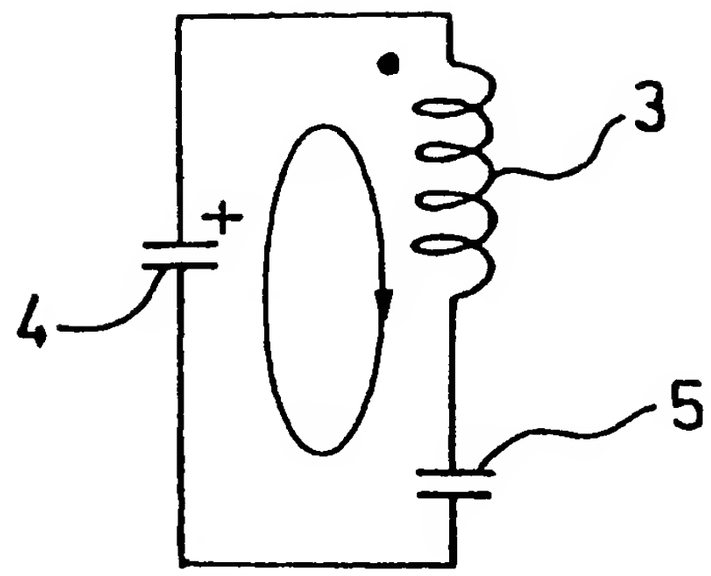


FIG. 3 (c)

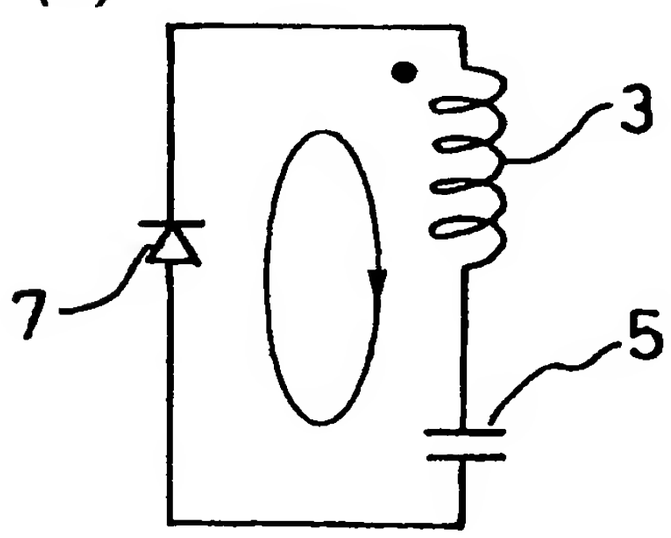


FIG. 3 (d)

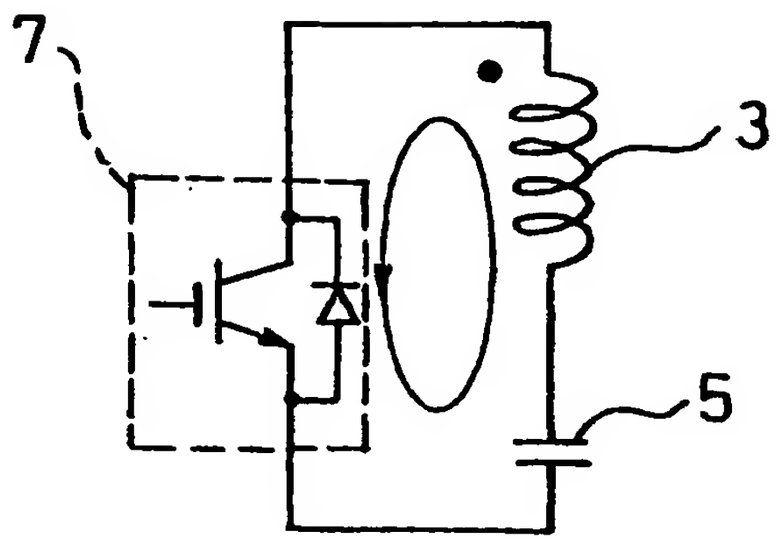


FIG. 3 (e)

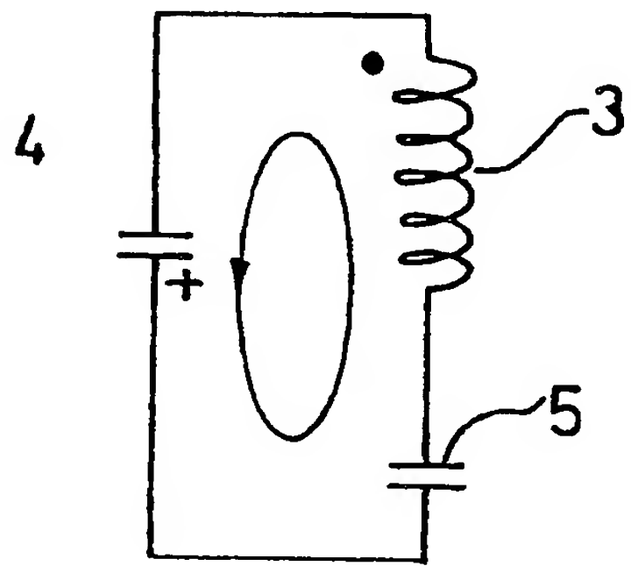


FIG. 3 (f)

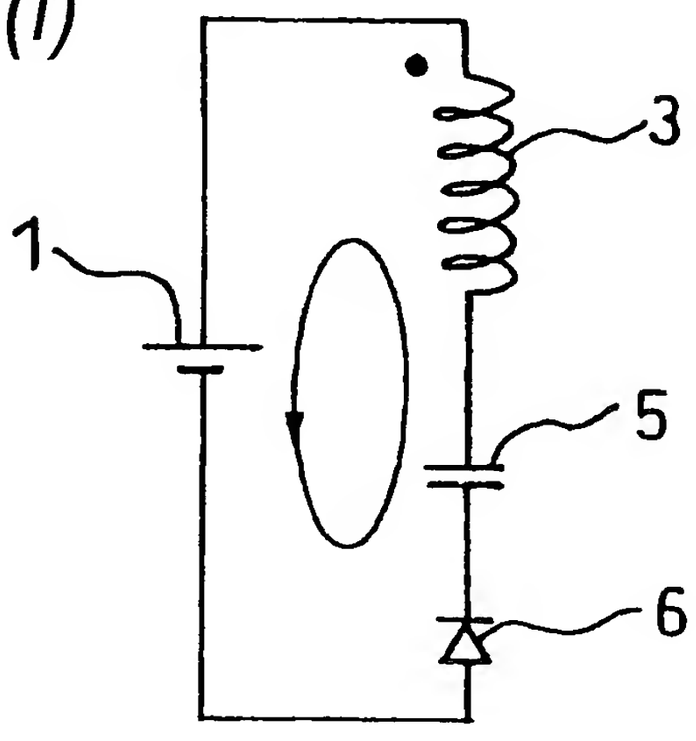


FIG. 4 (a) CURRENT OF FIRST SEMICONDUCTOR SWITCHING ELEMENT 6

FIG. 4 (b) VOLTAGE OF FIRST SEMICONDUCTOR SWITCHING ELEMENT 6

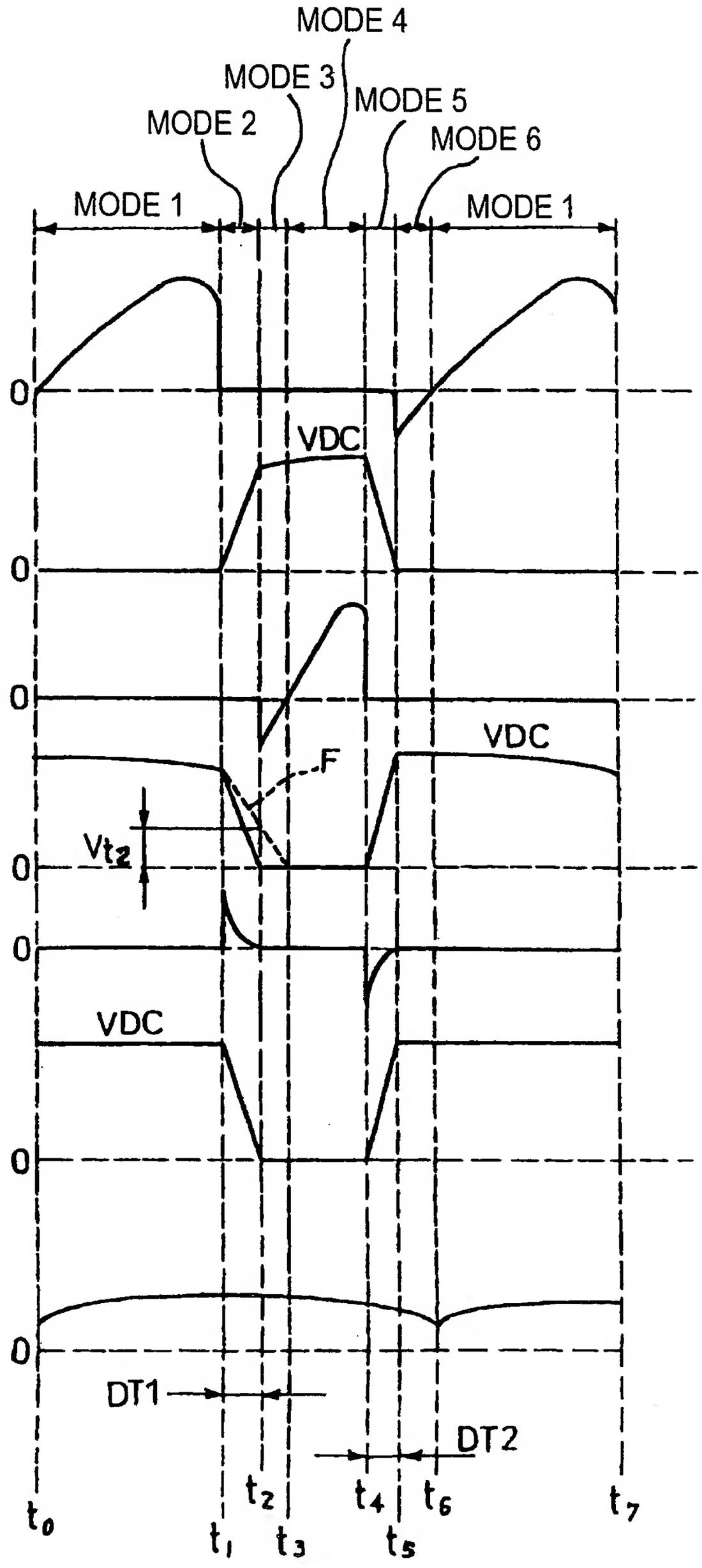
FIG. 4 (c) CURRENT OF SECOND SEMICONDUCTOR SWITCHING ELEMENT 7

FIG. 4 (d) VOLTAGE OF SECOND SEMICONDUCTOR SWITCHING ELEMENT 7

FIG. 4 (e) CURRENT OF FIRST CAPACITOR 4

FIG. 4 (f) VOLTAGE OF FIRST CAPACITOR 4

FIG. 4 (g) VOLTAGE OF SECOND CAPACITOR 5



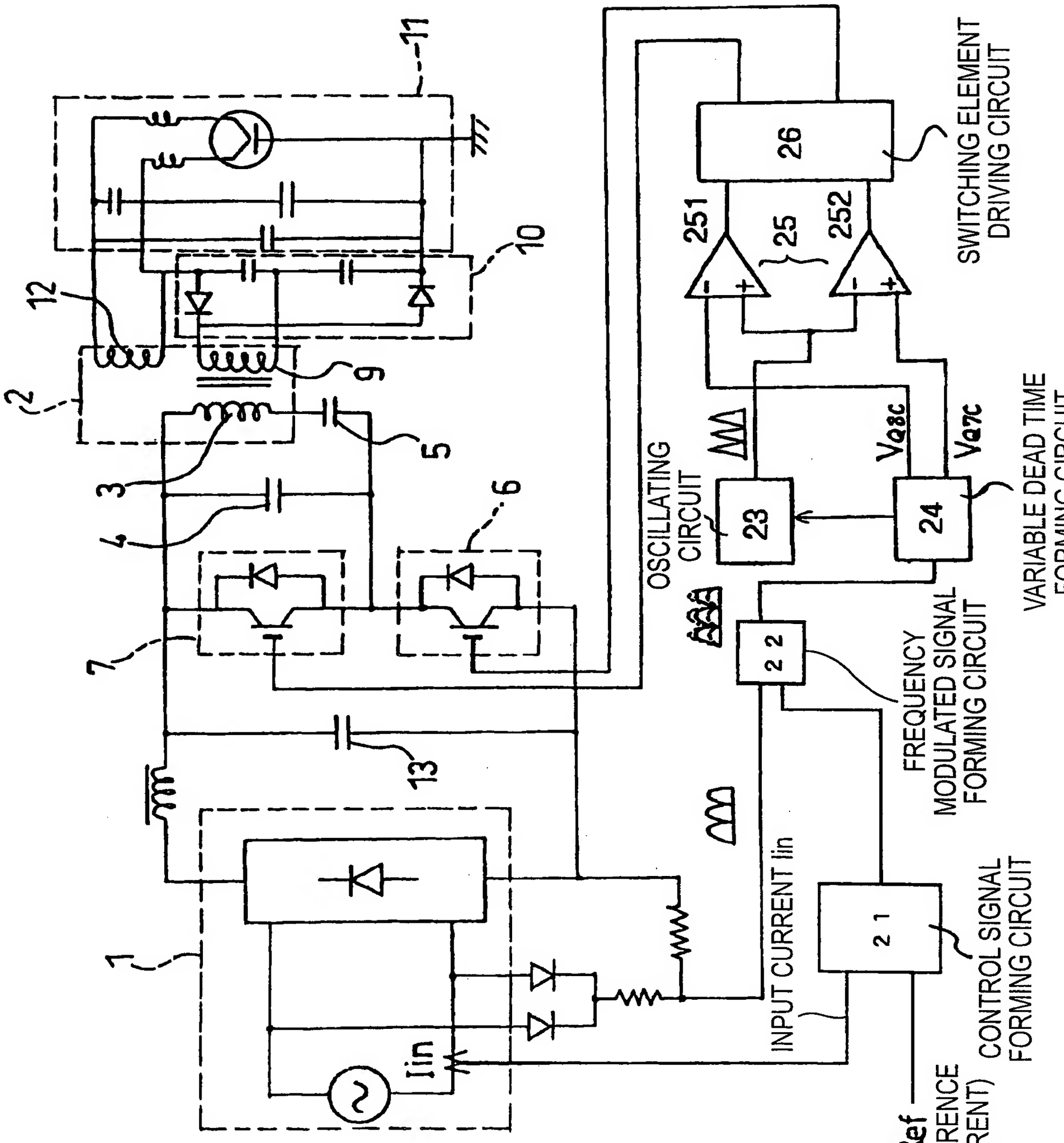

11
10
12
9
2
5
3
6
4
7
13
1
Iin
OSCILLATING CIRCUIT
SWITCHING ELEMENT DRIVING CIRCUIT
26
251
25
252
23
24
Vq3c
Vq7c
22
FREQUENCY MODULATED SIGNAL FORMING CIRCUIT
VARIABLE DEAD TIME FORMING CIRCUIT
INPUT CURRENT Iin
21
Ref
(REFERENCE CURRENT)
CONTROL SIGNAL FORMING CIRCUIT

FIG. 5

FIG. 6 (b)

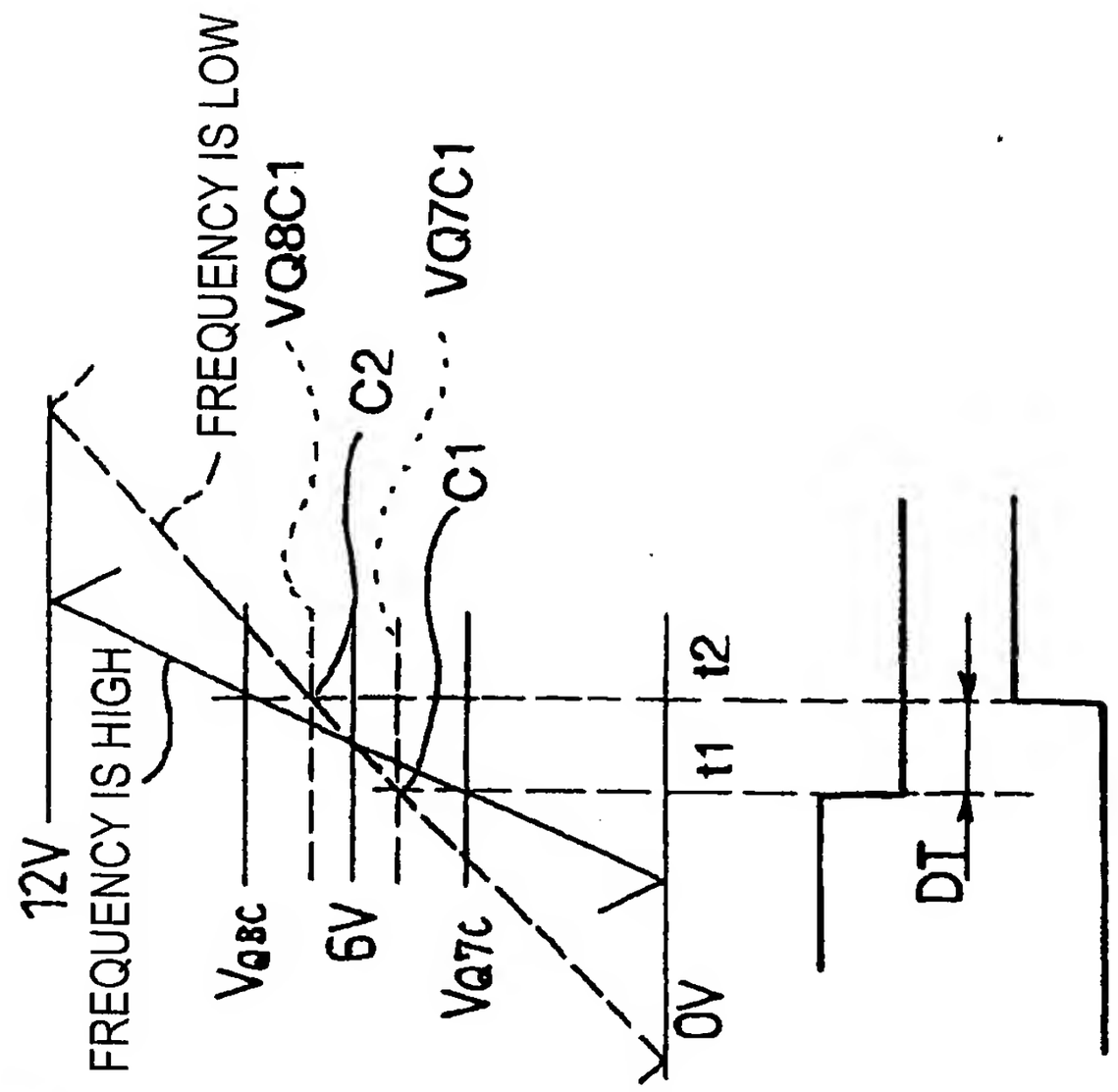
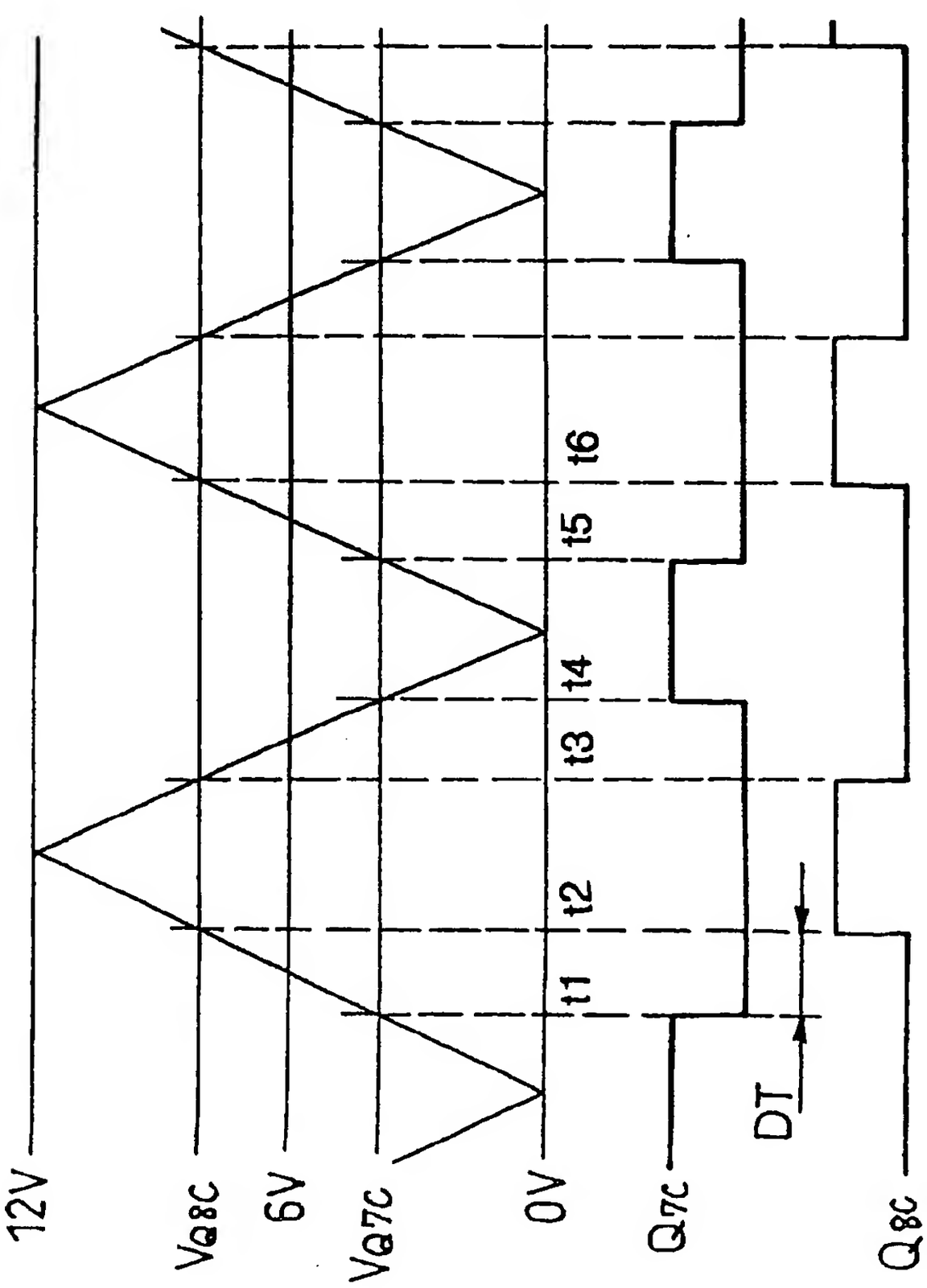

FREQUENCY IS LOW
VQ8C1
C2
VQ7C1
C1
12V
FREQUENCY IS HIGH
VQ8C
6V
VQ7C
0V
t1
t2
DT

FIG. 6 (a)


t6
t5
t4
t3
t2
t1
12V
VQ8C
6V
VQ7C
0V
DT
Q7C
Q8C

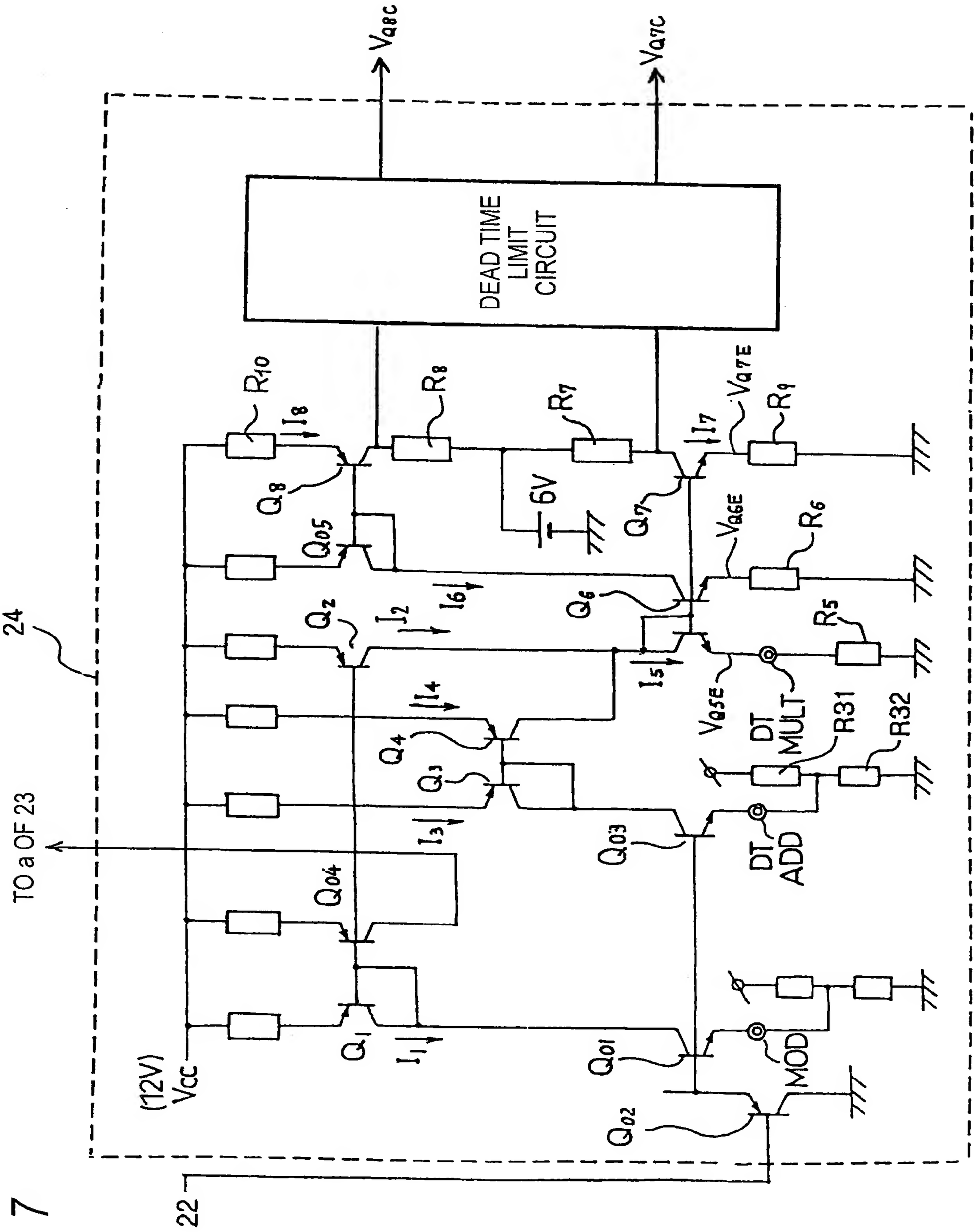
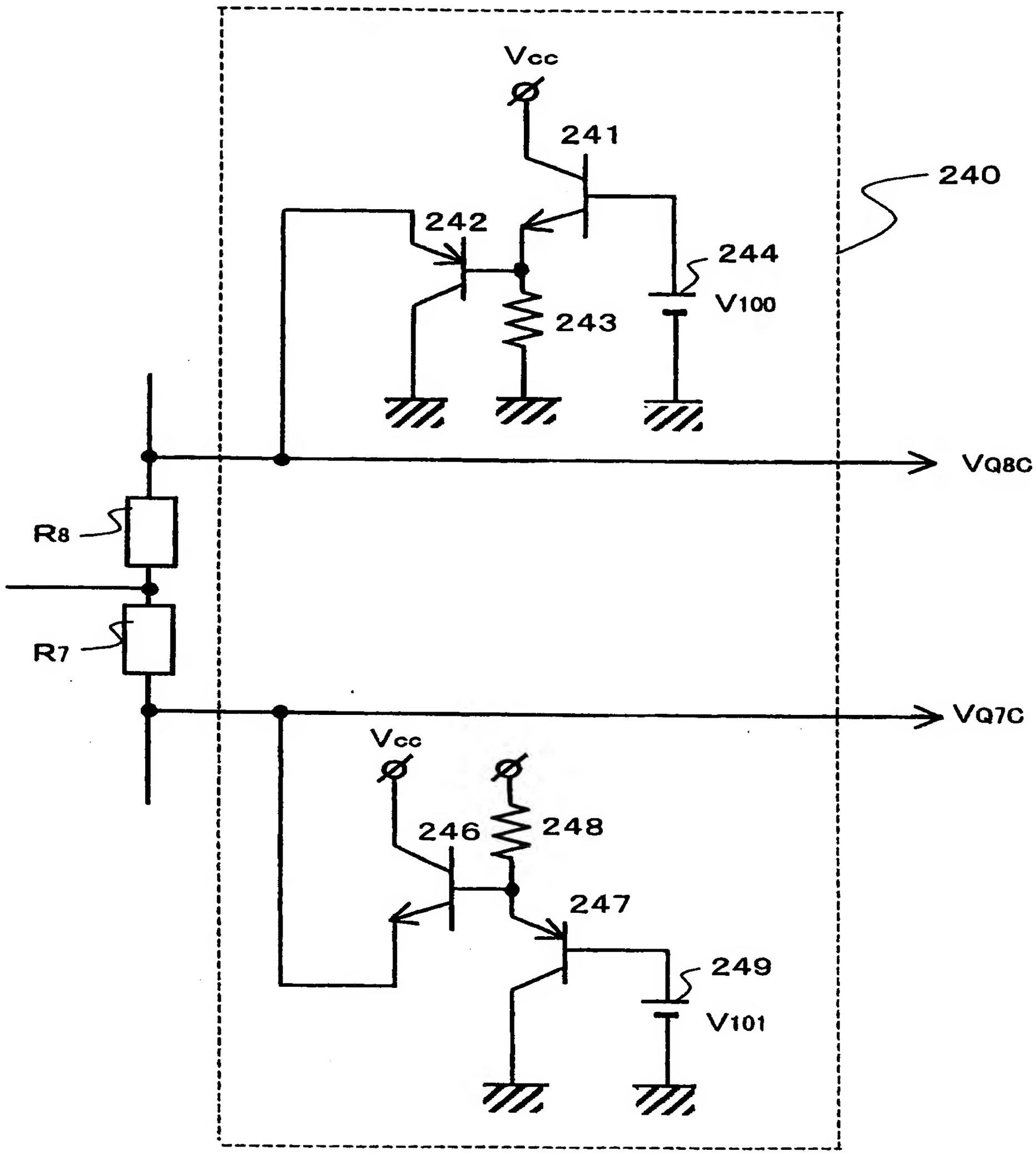

V_{Q8C}
V_{Q7C}
DEAD TIME LIMIT CIRCUIT
24
TO a OF 23
R_{10}
I_8
R_8
R_7
I_7
V_{Q7E}
R_9
Q_8
Q_{05}
6V
Q_7
V_{Q6E}
R_6
Q_2
I_2
I_6
Q_6
R_5
I_5
I_4
Q_4
Q_3
V_{Q5E}
DT MULT
R31
R32
I_3
Q_{04}
Q_{03}
DT ADD
(12V) Vcc
Q_1
I_1
Q_{01}
MOD
Q_{02}
22

FIG. 7

FIG. 8



(1) $V_{100} \neq V_{101}$

(2) $V_{100} < 12V$

FIG. 9

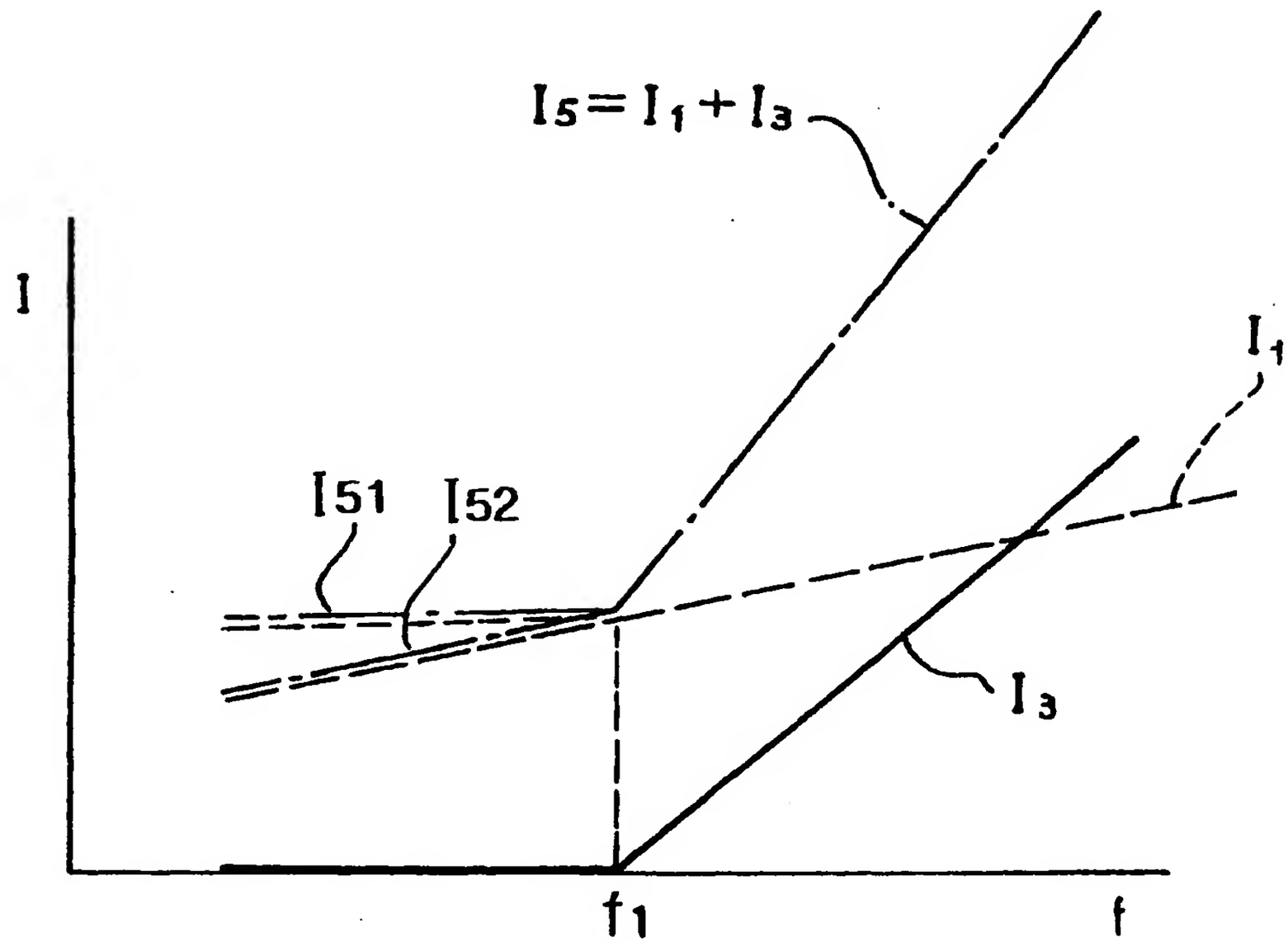


FIG. 10 (a)

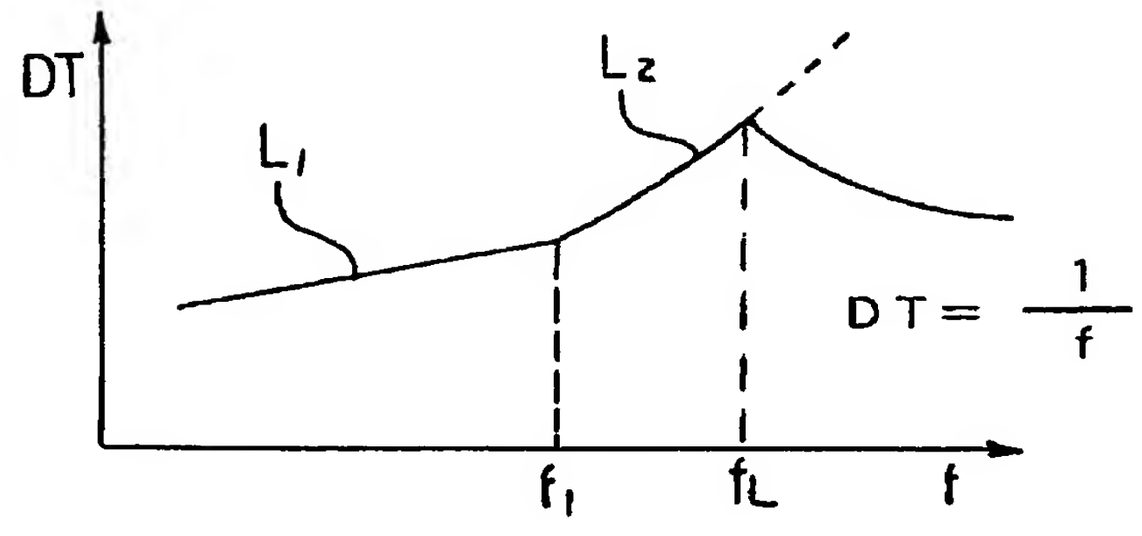


FIG. 10 (b1)

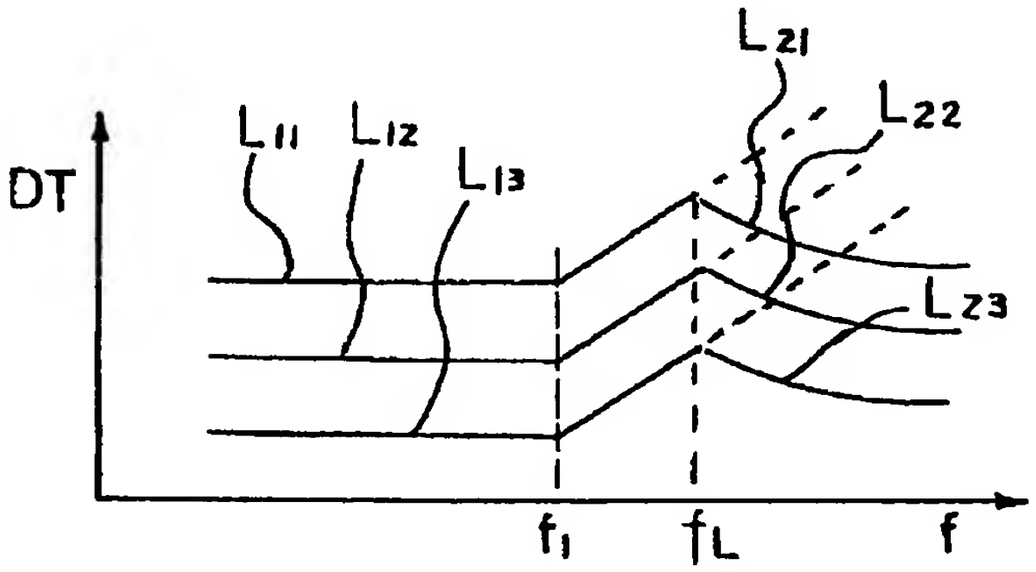


FIG. 10 (b2)

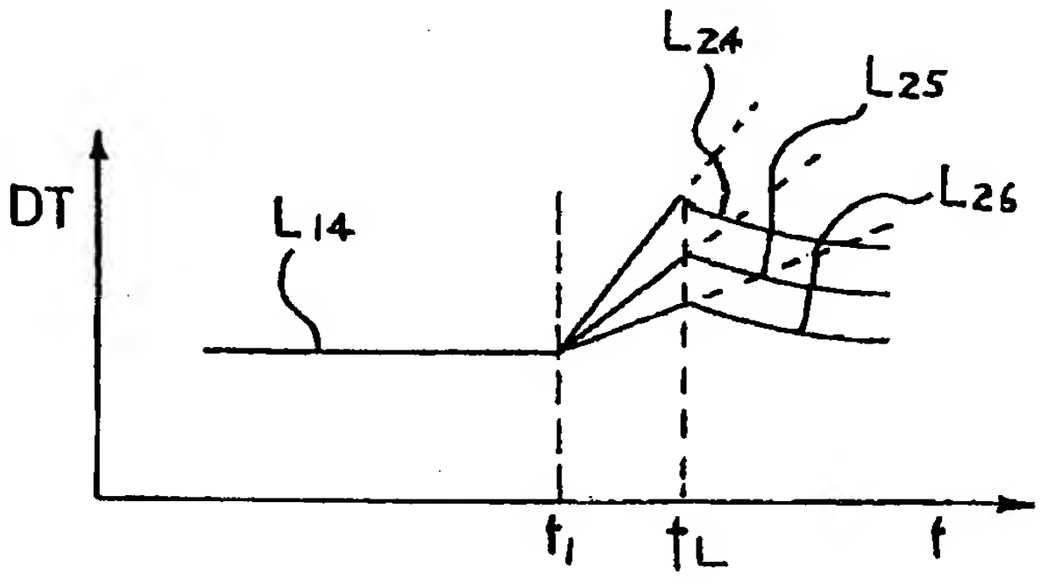


FIG. 10 (b3)

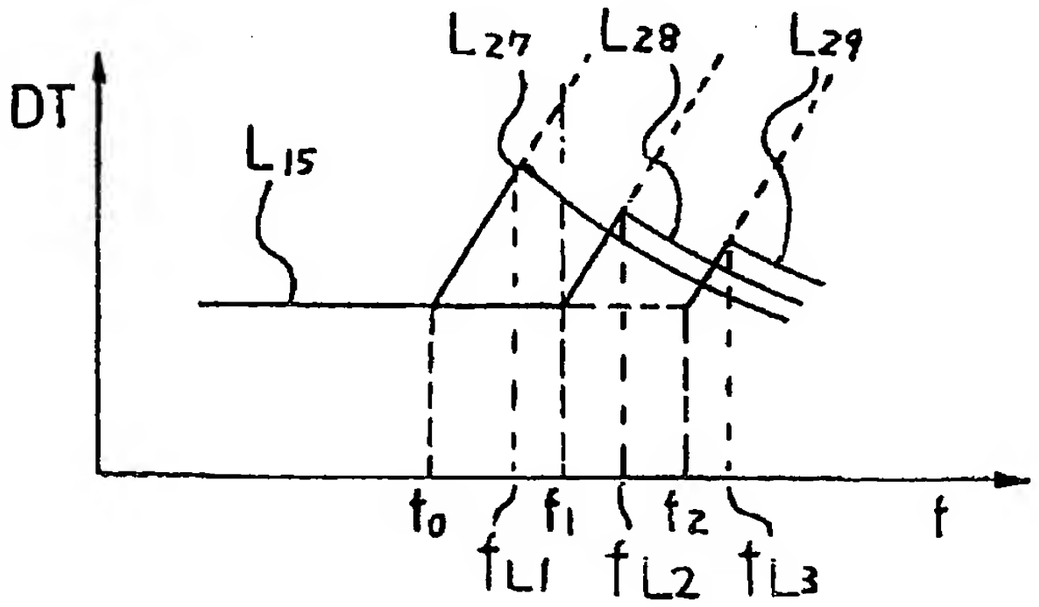


FIG. 11

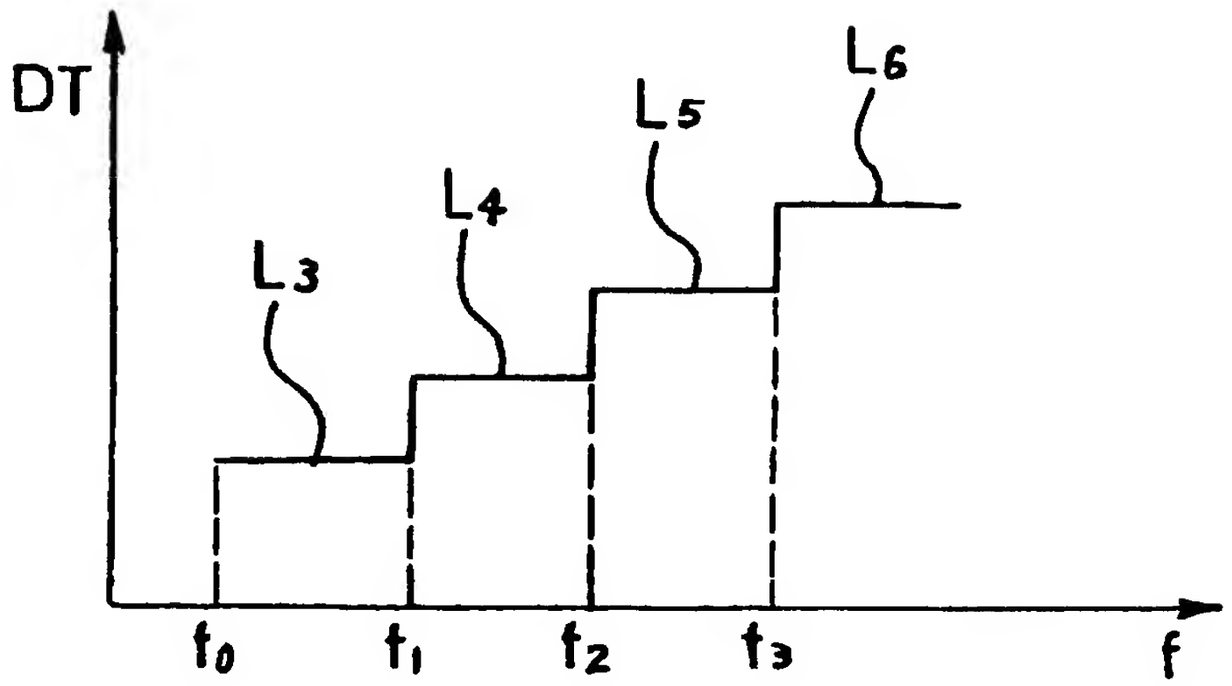


FIG. 12

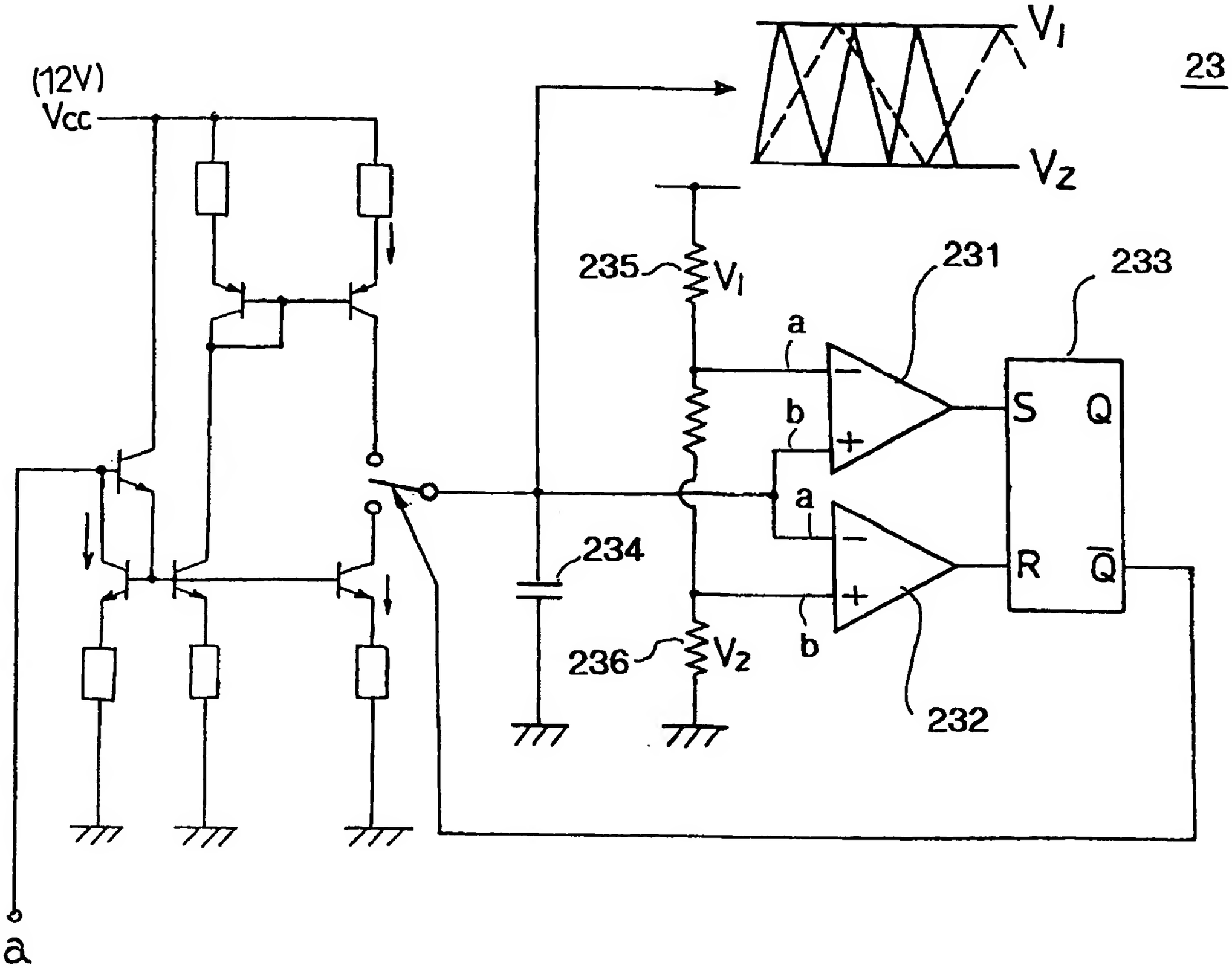

(12V)
Vcc
V_1
V_2
23
235
V_1
231
233
a
b
S
Q
a
234
R
$\overline{Q}$
236
V_2
b
232
a

FIG. 13 (a)

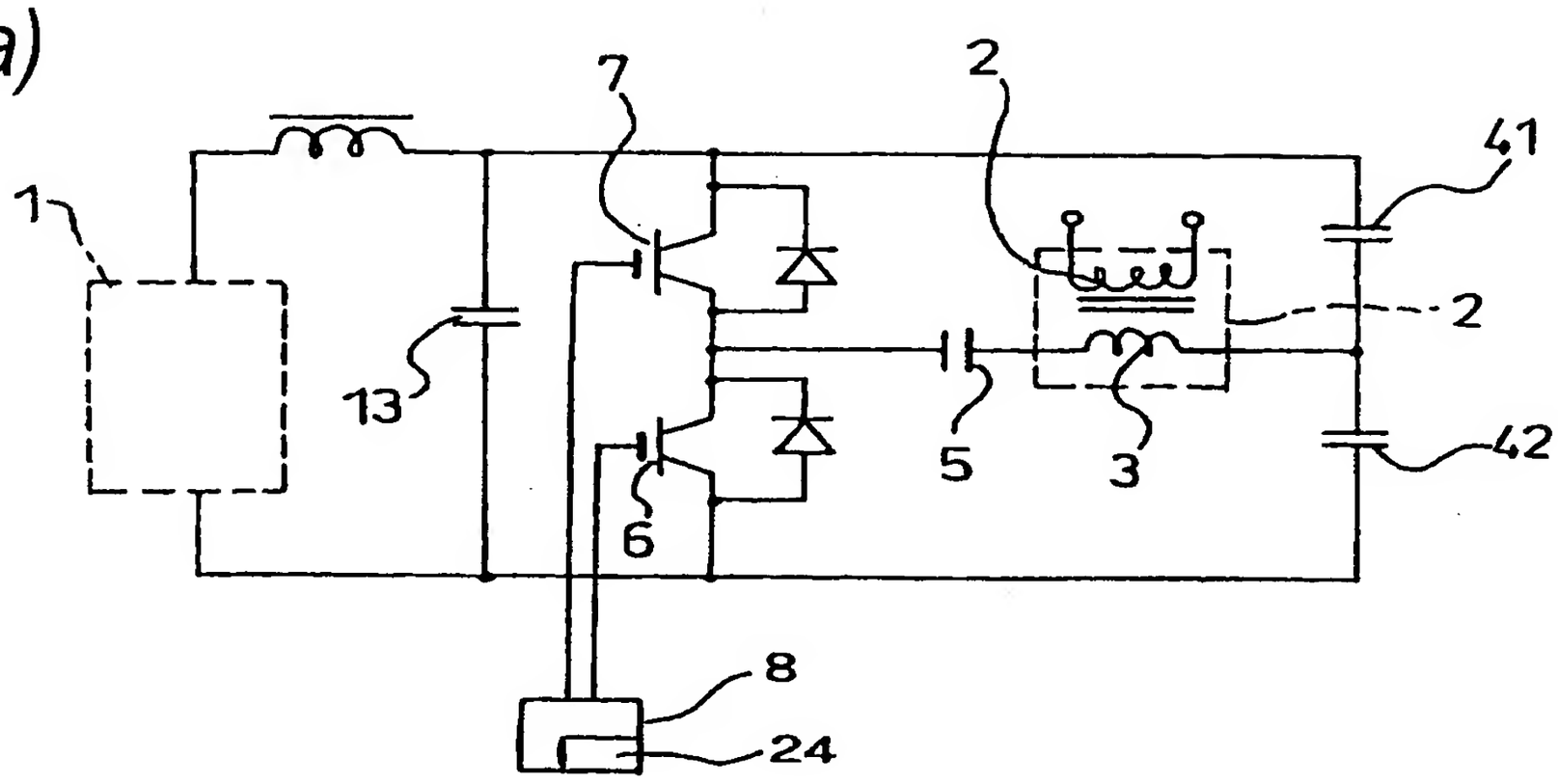


FIG. 13 (b)

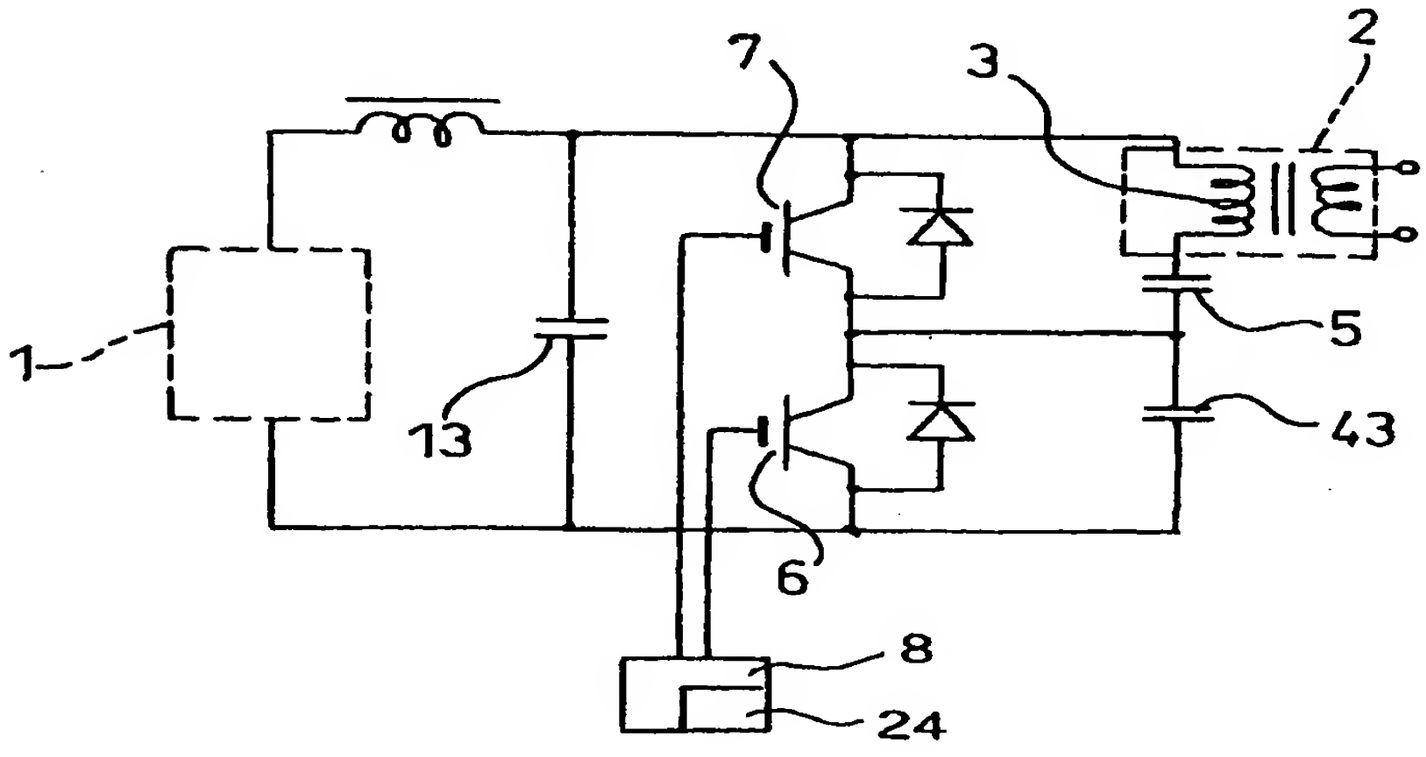


FIG. 13 (c)

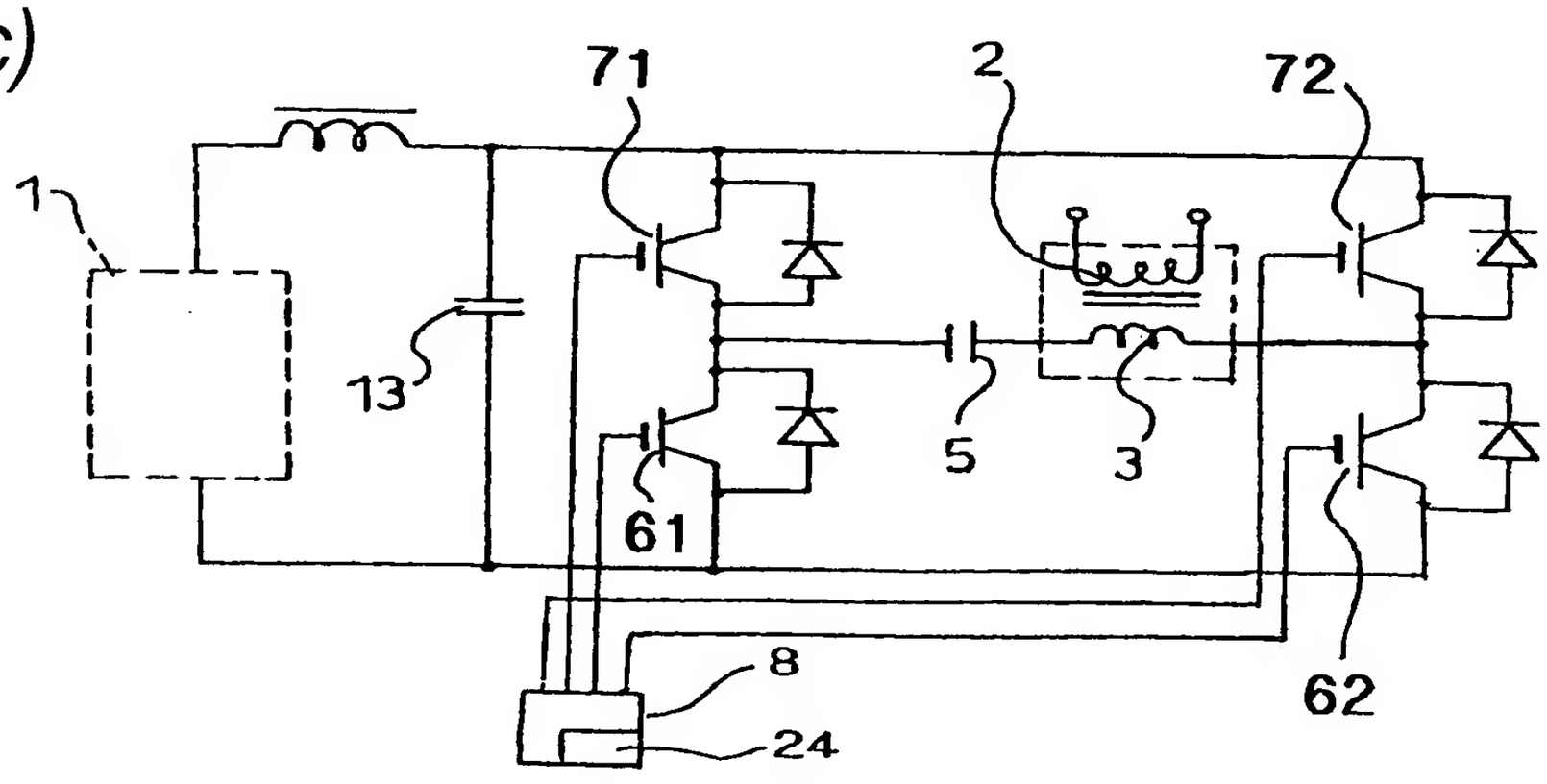


FIG. 14

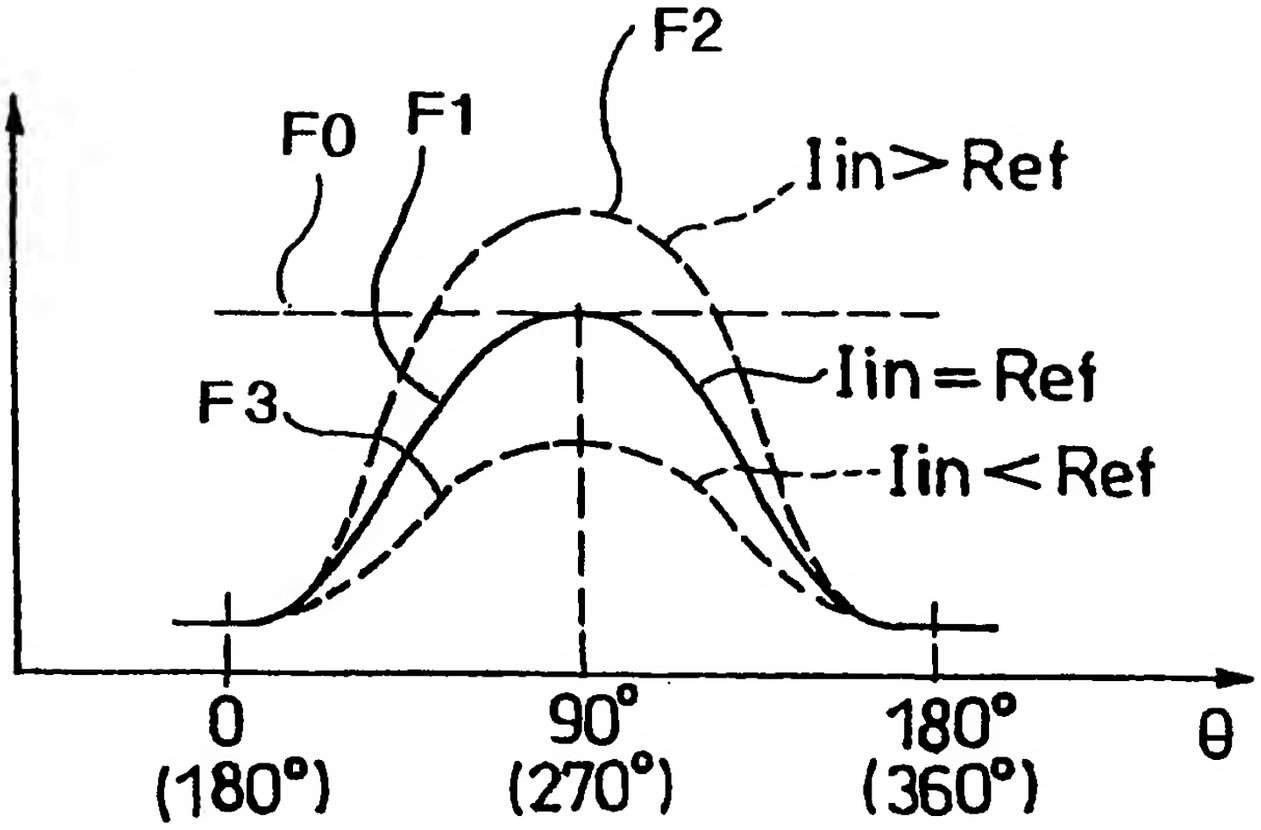
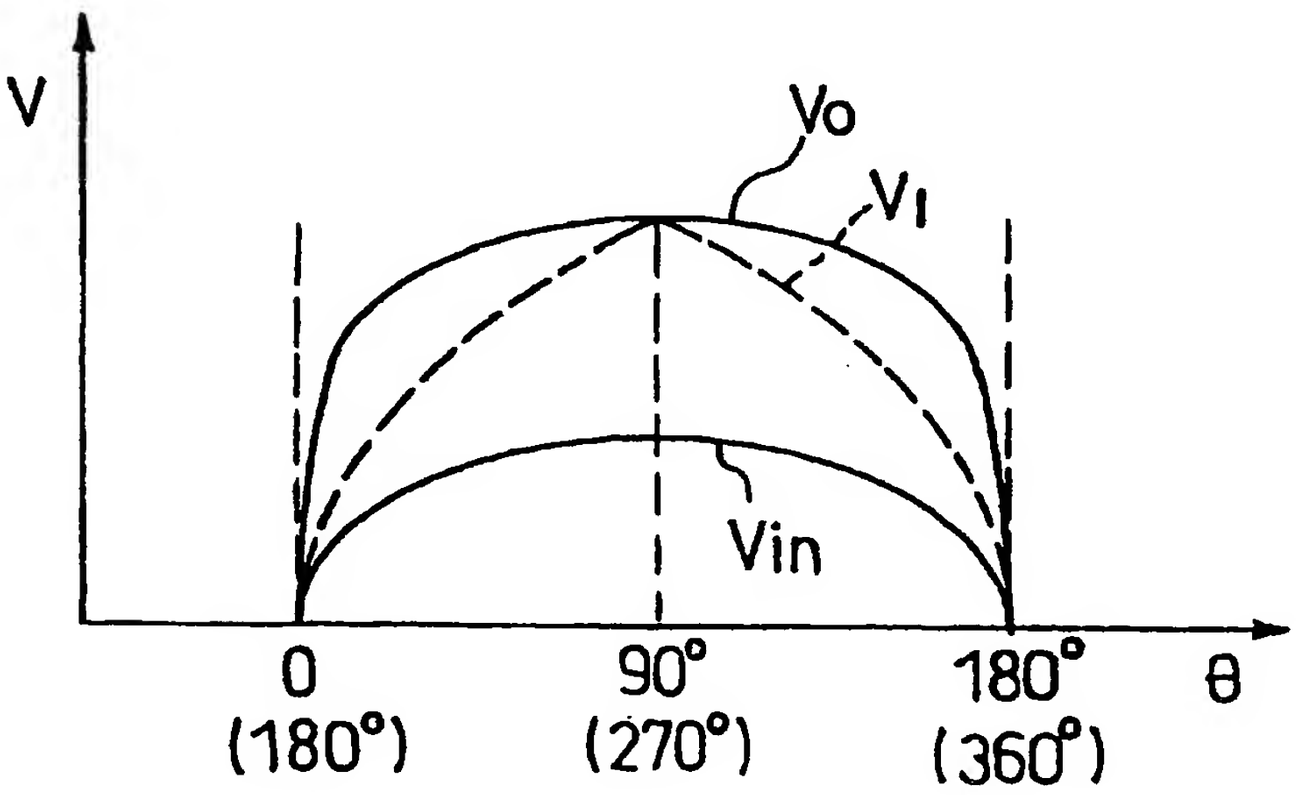

f
F0
F1
F2
Iin>Ref
Iin=Ref
Iin<Ref
F3
0
(180°)
90°
(270°)
180°
(360°)
θ

FIG. 15


V
Vo
V1
Vin
0
(180°)
90°
(270°)
180°
(360°)
θ